REMARKS

After entry of this amendment, claims 1 and 3 - 16 will be pending. Claims 1, 3 - 5, 7, 9, 11, 12, 13, 15, and 16 have been amended to clarify the scope of these claims. Support for the amendments may be found in the originally filed application in, e.g., the originally filed claims and Figure 4a and related text. No new matter has been added.

Objections to Specification

The Examiner objected to the title of the invention, the abstract, and an informality in the specification. Applicants addressed these objections by making appropriate amendments to the specification.

Objections to Claims

The Examiner objected to claims 11, 12, 15, and 16. Applicants have amended the claims accordingly.

Rejection of claims under 35 U.S.C. § 102

Claims 1, 2, 4, 13, and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,455,905 to Perugupalli et al. ("Perugupalli"). Perugupalli appears to disclose a push-pull transistor having first and second LDMOS transistors formed thereon and configured for push-pull operation, the first and second transistors sharing a common element current region. In a power transistor package, the push-pull transistor chip is attached to a mounting flange serving as a common element ground reference. *See* Perugupalli, abstract.

The Examiner relies on Perugupalli to teach all of the elements of independent claims 1 and 13. Peruguappalli, however, does not teach or suggest a structure including a first pair of devices and a second pair of devices, each pair of devices having a first source and a second source, such that both first source terminals are connected to both second source terminals to define a common source terminal, with each source terminal terminating on the first surface of a semiconductor substrate, as recited in amended independent claim 1. Perugupalli also does not teach or suggest a structure including two pairs of devices, with a first electrically isolated lead comprising both first source terminals connected to both second source terminals, with each source terminal terminating on the first surface of a semiconductor substrate, as recited in amended independent claim 13.

Rather, Perugupalli appears to describe discrete transistors that include source regions coupled to the surface of the flange. *See*, e.g., Figures 8 and 11 and related text. A common source region 155 is mentioned with respect to Figure 6, but this common source region appears to be a single source shared by two transistors, rather than two source terminals connected to each other, as required by claims 1 and 13.

Applicants submit that, for at least these reasons, amended independent claims 1 and 13 and claims dependent therefrom are patentable over the cited art.

Claims 1 and 3 – 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,389,810 to Agata et al. ("Agata"). Agata appears to disclose a semiconductor device having at least one symmetrical pair of MOSFETs, with each pair including a source region that is shared by the pair of MOSFETS. *See* abstract.

The Examiner relies on Agata to teach all of the limitations of independent claims 1 and 7. Agata, however, does not teach or suggest a structure including two pairs of devices, with the drain of the first device being connected to the drain of the second device and the gate of the first device being connected to the gate of the second device, as required by amended independent claims 1 and 7. Rather, Agata discloses devices with drains and gates that are isolated from each other, respectively. *See* Figures 11and 12 of Agata, and related text.

Applicants submit that, for at least this reason, amended independent claims 1 and 7 and claims dependent therefrom are patentable over the cited art.

Claims 9 and 10 are rejected under 35 U.S. C. § 102(b) as being anticipated by U.S. Patent Publication No. US 2002/0175373 to Utsunomiya et al. ("Utsunomiya"). Utsunomiya appears to disclose a semiconductor device which includes a pair of differential MOSFETs. The two sources 301 of the pair of MOSFETs appear to be connected to a common node 103. *See* Figure 4a of Utsunomiya, and related text.

The Examiner relies on Utsunomiya to teach all of the limitations of independent claim 9. Utsunomiya, however, does not teach or suggest two pairs of power transistor devices, with an electrically isolated lead comprising two first source terminals connected to both second source terminals, as recited in amended independent claim 9. In particular, Utsunomiya does not teach connecting the sources from two pairs of transistors to each other. Rather, Utsunomiya's devices

include discrete transistor pairs, with the sources within each pair of transistors being connected. *See*, e.g., Figure 4 of Utsunomiya, and related text. One of skill in the art would not combine these transistor pairs with each other, as the transistors disclosed by Utsunomiya appear to be suitable for conventional integrated circuits. *See*, e.g.., paragraphs [0041] – [0042] of Utsunomiya. Integrated circuit components are generally kept to a minimum, to reduce consumption of chip real estate. Power transistors, however, are preferably combined to increase the amount of power provided by a device.

Applicants submit that, for at least this reason, amended independent claims 9 and claims dependent therefrom are patentable over the cited art.

Rejection of claims under 35 U.S.C. § 103

Claims 11 and 12 are rejected under 35 U.S.C. § 103 as unpatentable over Utsunomiya in view of U.S. Patent No. 4,472,871 to Green et al. ("Green"). Applicants submit that these dependent claims are patentable for at least the reasons that independent claim 9, on which they depend, is patentable.

Claims 15 and 16 are rejected under 35 U.S.C. § 103 as unpatentable over Perugupalli in view of Green. Applicants submit that these dependent claims are patentable for at least the reasons that independent claim 13, on which they depend, is patentable.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

Applicants believe that no fees are necessitated by the present paper. However, in the event that any fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' attorney would expedite allowance of this application, the Examiner is cordially invited to call the undersigned attorney at (617) 570-1806.

Respectfully submitted,

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Reg. No. 44,381

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